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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,624	09/30/2003	William M. Siu	042390P6107D	7830

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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 08/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/676,624	SIU ET AL.	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *28-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *28-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09-30-03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. **NON-STATUTORY**

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 28-41 are rejected under the judicially created doctrine of 0bviousness-type double patenting as being unpatentable over claims 1-14 of U.S. Patent No. 6664620 (Siu et al.) in view of Brandenburg et al. (US Pat. 5491364).

A. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 1 of U.S. Patent No. 6664620 (Siu et al.) includes a semiconductor package/apparatus comprising:

- a substrate having a surface, said surface having a central region and an outer region
- a first plurality of rows of electrical connections on said surface, each of said rows extending from the central region to the outer region
- wherein a space between every pair of adjacent rows of the first plurality of rows is progressively larger from the central region to the outer region to contain progressively increasing number of conductive traces, the space containing no electrical connections, and
-wherein none of the electrical connections in each row are directly connected to one another electrically.

Regarding claim 28, claim 1 of Siu et al. fail to teach a printed circuit board (PCB) functioning as the package/apparatus.

Brandenburg et al. teach a semiconductor package comprising a PCB substrate having a plurality of electrical connections (see 14 in Fig. 1 and 4; Col. 2; Col.1 –6).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the PCB comprising the substrate as taught by Brandenburg et al. so that the desired circuit connections and routing can be achieved in Siu et al's structure.

Regarding claim 29, claim 2 of Siu et al. substantially teaches the entire claimed structure as applied to claim 28 above, including the electrical connections being selected from a group comprising input/output connections, power connections, and ground connections.

Regarding claim 30, claim 3 of Siu et al. substantially teaches the entire claimed structure as applied to claim 28 above, including the electrical connections comprising an array of electrically conductive bumps.

Regarding claim 31, claim 4 of Siu et al. substantially teaches the entire claimed structure as applied to claim 28 above, including a semiconductor die being coupled to the substrate and having a second plurality of rows of electrical connections positioned

to match the first plurality of rows of electrical connections responsive to the semiconductor die being coupled to the substrate.

Regarding claim 32, claim 5 of Siu et al. substantially teaches the entire claimed structure as applied to claim 28 above, including each of the rows extending radially from the central region to the outer region.

B. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 6 of U.S. Patent No. 6664620 (Siu et al.) includes a semiconductor package/apparatus comprising:

- an integrated circuit die having a surface, said surface having a central region and an outer region
- a first plurality of rows of electrical connections on said surface, each of said rows extending from the central region to the outer region
- a space between each adjacent row, each of the spaces containing no electrical connections, and
- wherein an average of all the spaces is progressively non-decreasing from the central region to the outer region.

Regarding claim 33, claim 6 of Siu et al. fail to teach a device functioning as the package/apparatus.

Brandenburg et al. teach a semiconductor device/package/a PCB substrate having a plurality of electrical connections (see 14 in Fig. 1 and 4; Col. 2; Col.1 –6).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the device comprising the substrate as taught by Brandenburg et al. so that the desired device/circuit connections and routing can be achieved in Siu et al's structure.

Regarding claim 34, claim 7 of Siu et al. substantially teaches the entire claimed structure as applied to claim 33 above, including the average of all the spaces being progressively increasing from the central region to the outer region.

Regarding claim 35, claim 8 of Siu et al. substantially teaches the entire claimed structure as applied to claim 33 above, including the electrical connections comprising an array of electrically conductive bumps.

Regarding claim 36, claim 9 of Siu et al. substantially teaches the entire claimed structure as applied to claim 33 above, including the first plurality of rows of electrical connections being positioned on said surface in a pattern to match a second plurality of rows of electrical connections on a substrate responsive to the integrated circuit die being coupled to said substrate.

Regarding claim 37, claim 10 of Siu et al. substantially teaches the entire claimed structure as applied to claim 33 above, including each of said rows extending radially from the central region to the outer region.

C. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 11 of U.S. Patent No. 6664620 (Siu et al.) includes a semiconductor package/apparatus comprising:

-a substrate having a first surface, said first surface having a central region and an outer region

- a first plurality of rows of electrical connections on said first surface, each of said rows extending from the central region to the outer region, wherein a space between ones of the electrical connections at substantially a same distance from the central region of the first plurality of rows is progressively larger from the central region to the outer region, said space containing no electrical connections; and

- a semiconductor die coupled to the substrate and having a second plurality of rows of electrical connections.

Regarding claim 38, claim 11 of Siu et al. fail to teach a printed circuit board (PCB) functioning as the package/apparatus.

Brandenburg et al. teach a semiconductor package comprising a PCB substrate having a plurality of electrical connections (see 14 in Fig. 1 and 4; Col. 2; Col.1 –6).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the PCB comprising the substrate as taught by Brandenburg et al. so that the desired circuit connections and routing can be achieved in Siu et al's structure.

Regarding claim 39, claim 12 of Siu et al. substantially teaches the entire claimed structure as applied to claim 38 above, including the space between adjacent rows of the first plurality of rows being progressively increasing from the central region to the outer region.

Regarding claim 40, claim 13 of Siu et al. substantially teaches the entire claimed structure as applied to claim 38 above, including the first plurality of rows of electrical connections being positioned on said surface in a pattern to match the second plurality of rows of electrical connections responsive to the semiconductor die being coupled to the substrate.

Regarding claim 41, claim 13 of Siu et al. substantially teaches the entire claimed structure as applied to claim 38 above, including each of the rows extending radially from the central region to the outer region.

Response to Arguments

3. Applicant's arguments with respect to claims 28-41 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's acting supervisor, Steven Loke can be reached on 571-272-1657. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAN or Public PAG. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAG system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

NP

08-07-05

NITIN PAREKH

PRIMARY EXAMINER

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